Claims

1. A method for operating a memory cell that is capable of storing multiple levels of charge, comprising:

programming the memory cell from each of a right side and a left side, the right side capable of storing a right bit and the left side capable of storing a left bit, a quantity of charge used in the programming of the memory cell setting when interaction between the right bit and the left bit is to exist; and

reading a charge level of the memory cell from a single side of the memory cell.

2. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein reading the charge level from the single side limits reading from one side of the memory cell to enable identification of the charge level.

3. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein the reading enables identification of the charge level when a read voltage is applied to a diffusion terminal of the single side of the memory cell and a ground voltage is applied to a diffusion terminal of the opposite side of the single side.

4. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 3, wherein the read voltage is maintained below 2 volts.

5. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein the interaction between the right bit and the left bit exists when a higher charge is stored in the memory cell relative to lower charges that do not cause interaction between the right bit and the left bit.

6. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 5, wherein four, eight, and sixteen memory states of the memory cell can be achieved through the combination of the right bit, the left bit, the quantity of charge, and the charge position.

7. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein increased programmed charge in the left bit causes the interaction between the right bit and the left bit, such that the right bit is induced to increase in correlation with increases in the programmed charge in the left bit.

8. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein higher threshold voltages of the memory cell can be achieved when the interaction between the right bit and the left bit of the memory cell exists relative to lower threshold voltages of the memory cell when no interaction between the right bit and the left bit of the memory cell exists.

9. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein the memory cell is a NROM cell.

10. A method for operating a memory cell that is capable of storing multiple levels of charge, comprising:

programming the memory cell from each of a first side and a second side, the first side capable of storing a first bit and the second side capable of storing a second bit, a quantity of charge used in the programming of the memory cell setting when interaction between the first bit and the second bit exists, and

reading a charge level of the memory cell from a single side of the memory cell.

11. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 10, wherein the first side is a right side and the first bit is a right bit, and the second side is a left side and a second bit is a left bit.

12. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein reading the charge level from the single side limits reading from one side of the memory cell to enable identification of the charge level.

13. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein the reading enables

identification of the charge level when a read voltage is applied to a diffusion terminal of the single side of the memory cell and a ground voltage is applied to a diffusion terminal of the opposite side of the single side.

14. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 13, wherein the read voltage is maintained below 2 volts.

15. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein the interaction between the right bit and the left bit exists when a higher charge is stored in the memory cell relative to lower charge that do not cause interaction between the right bit and the left bit.

16. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 15, wherein four, eight, and sixteen memory states of the memory cell can be achieved through the combination of the right bit, the left bit, the quantity of charge, and the charge position.

17. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein increased programmed charge in the right bit causes the interaction between the right bit and the left bit, such that the left bit is induced to increase in correlation with increases in the programmed charge in the right bit.

18. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein higher threshold voltages of the memory cell can be achieved when the interaction between the right bit and the left bit of the memory cell exists relative to lower threshold voltages of the memory cell when no interaction between the right bit and the left bit of the memory cell exists.

19. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein the memory cell is a NROM cell.

20. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 10, wherein the first side is a left side and the first bit is a left bit, and the second side is a right side and a second bit is a right bit.

21. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein reading the charge level from the single side limits reading from one side of the memory cell to enable identification of the charge level.

22. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein the reading enables identification of the charge level when a read voltage is applied to a diffusion terminal

of the single side of the memory cell and a ground voltage is applied to a diffusion terminal of the opposite side of the single side.

23. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 22, wherein the read voltage is maintained below 2 volts.

24. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein the interaction between the right bit and the left bit exists when a higher charge is stored in the memory cell relative to lower charge that do not cause interaction between the right bit and the left bit.

25. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 24, wherein four, eight, and sixteen memory states of the memory cell can be achieved through the combination of the right bit, the left bit, the quantity of charge, and the charge position.

26. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein increased programmed charge in the right bit causes the interaction between the right bit and the left bit, such that the left bit is induced to increase in correlation with increases in the programmed charge in the right bit.

27. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein higher threshold voltages of the memory cell can be achieved when the interaction between the right bit and the left bit of the memory cell exists relative to lower threshold voltages of the memory cell when no interaction between the right bit and the left bit of the memory cell exists.

28. The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein the memory cell is a NROM cell.

29. A semiconductor memory cell, the memory cell being capable of storing multiple levels of charge, comprising:

a first programmed side defined by an applied programming voltage at a first side of the memory cell and a ground of a second side of the memory cell;

a second programmed side defined by an applied a programming voltage at the second side of the memory cell and a ground of the first side of the memory cell; and

a single read side defined by an applied read voltage of the first side of the memory cell and a ground of the second side of the memory cell.